REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995

Application Number	09/980,098
Confirmation Number	1120
Filing Date	November 29, 2001
First Named Inventor	Shinji ITAMI
Group Art Unit	2112
Examiner Name	Christopher E. LEE
Matter Number	Q67475
Title	DATA TRANSMISSION SYSTEM

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

1. SUBMISSION REQUIRED UNDER 37 C.F.R. § 1.114

a. ☑ Previously submitted
   i. ☑ Please enter and consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on March 3, 2005
   ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
   iii. ☐ Other _____

b. ☑ Enclosed
   i. ☑ Amendment/Reply
   ii. ☐ Affidavit(s)/Declaration(s)
   iii. ☐ Information Disclosure Statements (IDS)
   iv. ☑ Petition for Extension of Time
   v. ☐ Other _____

2. MISCELLANEOUS

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months

b. ☐ Other _____

3. FEES

A check for the RCE statutory fee of $790.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this transmittal letter is attached.

CORRESPONDENCE ADDRESS

Direct all correspondence to the address for SUGHRUE MION, PLLC filed under the Customer Number listed below:

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

SIGNATURE OF ATTORNEY

Name Nataliya Dvorson Registration No. 56,616

Signature _____ Date April 4, 2005

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Shinji ITAMI

Appln. No.: 09/980,098

Confirmation No.: 1120

Filed: November 29, 2001

For: DATA TRANSMISSION SYSTEM

Docket No: Q67475

Group Art Unit: 2112

Examiner: Christopher E. LEE

AMENDMENT UNDER 37 C.F.R. § 1.114(c)

MAIL STOP RCE
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Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated December 3, 2005 and in supplement to the Amendment under 37 C.F.R. § 1.116 filed on March 3, 2005, please further amend the above-identified application as follows on the accompanying pages.

TABLE OF CONTENTS

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A data transmission system, comprising:

a primary board;

secondary boards; and

a data transmission path carrying out data transmission/reception between the primary board and the secondary boards, the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein when the data access is executed from the primary board to the secondary boards, informing a start address required for data access, and wherein an address used in the data access in the secondary boards is

generated based on the start address, a predetermined trigger signal and a cycle signal indicating switching of data, the cycle signal is combined with the trigger signal.

2. (canceled).

3. (original): The data transmission system according to claim 1, wherein, when the address is generated based on the trigger signal, the address is generated sequentially by incrementing the start address in response to a timing of the trigger signal.

4. (canceled).

5. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data transmission/reception between the primary board and the secondary boards, where the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein:

when the data access is executed from the primary board to the secondary boards, informing a memory start address of the secondary boards required for data access,

judging in the secondary boards whether or not the memory start address is directed to own station, and then executing the data transmission via the data transmission path by accessing a memory in own station based on the memory start address when the memory start address is directed to own station, and

an address is generated, to which the data transmission is subsequently executed, in the secondary boards by incrementing the memory start address after the data transmission based on the memory start address is ended, and then executing the data transmission via the data transmission path by accessing the memory of own station based on the generated address, ~~and~~

wherein a cycle signal indicating switching of data is used in combination with a trigger signal,

wherein the address is not incremented when a waveform is deformed by the trigger signal, and

wherein the second board does not shift to a next process until a phase has been toggled, and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the phase. ~~,~~

6. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data read between the primary board and the secondary boards, wherein the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein the data transmission system executes the following step in carrying out data transmission:

informs a trigger signal combined with a cycle signal indicating a timing of data access, and a start address required for data read via the data transmission path,

switches the data transmission path to which the start address is informed as a data bus,

accesses a memory based on the start address and sending out a read result onto the data transmission path, and

increments the start address at a timing of the trigger signal, and then sending out a read result onto the data transmission path by accessing the memory based on the incremented address,

wherein the address is not incremented when a waveform is deformed by the trigger signal, and

wherein the second board does not shift to a next process until a phase has been toggled, and leading and trailing edges of the trigger signal are detected in combination with detecting the toggle states of the phase.

7. (canceled).

8. (currently amended): A data transmission system comprising:

a primary board;

secondary boards; and

a data transmission path for carrying out data write between the primary board and the secondary boards, where the data transmission path employs a same signal line as an address bus and a data bus mutually,

wherein the carrying out of the data transmission/reception is executed by:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path,

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory, ~~and~~

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address,

detecting leading and trailing edges of the trigger signal in combination with detecting toggle states of a phase,

not incrementing the address when a waveform is deformed by the trigger signal, and

not shifting the second board to a next process until the phase has been toggled.

9. (canceled).

10. (previously presented): A method for carrying out data write between a primary board and secondary boards by using a data transmission path, which employs a same signal line as an address bus and a data bus mutually, comprising:

informing a trigger signal combined with a cycle signal indicating a timing of data access and a start address required for data write via the data transmission path;

switching the data transmission path to which the start address is informed as a data bus, and then sending out a predetermined data to be written to a memory;

accessing the memory based on the start address, and then writing the predetermined data into the memory; and

incrementing the start address at a timing of the trigger signal, and then writing sequentially the predetermined data, that are sent out via the data transmission path, into the memory by accessing the memory based on the incremented address.

REMARKS

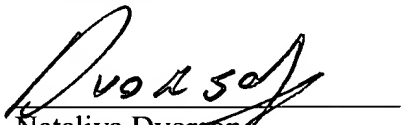
Upon entry of this Amendment, claims 1, 3, 5, 6, 8 and 10 are all the claims pending in the application. The Amendment under 37 C.F.R. § 1.116 filed on March 3, 2005 is entered in due to the attached Request for Continued Examination (RCE) filed concurrently herewith.

Applicant is further amending claims 5, 6, and 8 to clarify the invention. Specifically, claims 5, 6, and 8 are related to a technique to prevent malfunction of a multiplexer due to disturbance of a signal (trigger signal). The address is not changed only by the variation of the trigger signal, but is changed using the cycle signal in combination with the trigger signal. Therefore, the object of the present invention is different from that of Oshikawa, which is related to the multiplexer itself and not to prevention of malfunction via the unique features identified in claims 5, 6, and 8.

In view of the above, entry and consideration of this Amendment is respectfully requested. Moreover, allowance of this application is now believed to be in order, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: April 4, 2005

Attorney Docket No.: Q67475